

A MIPS Hazard Example
CPE 315
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Note: this is 16 bit code

This example assumes the CPU
a. pipeline doesn't use stalling
b. has hardware forwarding.

A hunk of C code

```
a = b + 1;  
if ( c != 0 )  
    d = 0;
```

Compiles "naturally" to:

```
lw   $2, b($0)  
nop                                     { Bubble needed even with forwarding }  
addi $2, $2, 1  
sw   $2, a($0)  
lw   $3, c($0)  
nop  
beq  $0,$3, skip                       { Note that beq requires 4 cycles }  
nop  
nop  
nop  
sw   $0, d($0)  
skip:
```

A MIPS compiler might generate

```
lw   $2, b($0)  
lw   $3, c($0)  
addi $2, $2, 1  
beq  $0, $3, skip  
sw   $2, a($0)  
nop  
nop  
sw   $0, d($0)  
skip:
```

This code can still be improved. See if you can eliminate one more instruction.