

CPE 315
 Winter 2008
 Exam #1 Answers

1.

$$\begin{array}{r} 78 \\ + 8A \\ \hline 02 = 02_{10} \end{array}$$

C = 1 and V = 0

Answer is correct if 2's complement, incorrect if unsigned

$$\begin{array}{r} 98 \\ - 8A \\ \hline 0E = 14_{10} \end{array}$$

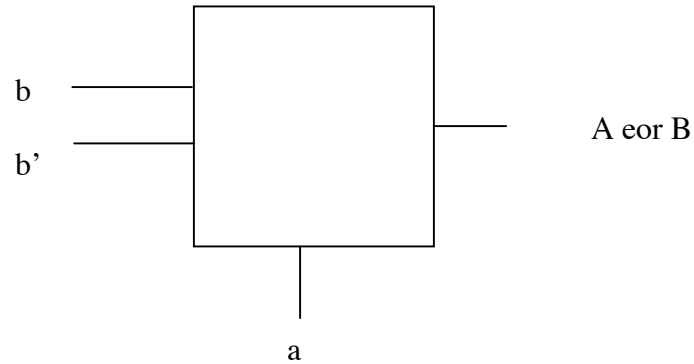
C = 1(wrong) and V = 0

Answer is correct if 2's complement, correct if unsigned

2. Ask in office hour/lab for bus coloring

	Bit 0	Bit 7
Ainvert	0	0
Binvert	1	1
Carryin	1	1
Operation	10	10
Result	0	0
Overflow	n/a	0
CarryOut	0	n/a
b	0	1
a	0	1

3.



4. Connect the Parity values to the eight Mux inputs and A,B,C to the Mux selects. This is the easiest possible way to implement any combinatorial logic circuit.

5. The PS/NS Table

D2	D1	D0	D2+	D1+	D0+
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	x	x	x
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	x	x	x
1	1	0	1	0	0
1	1	1	1	1	0

The equations. Minimization is easy by KMap or visual inspection.

$$D2+ = D2'D1D0 + D2D1D0' + D2D1D0 = D1$$

$$D1+ = D2'D1'D0 + D2'D1D0 + D2D1D0 = D0$$

$$D0+ = D2'D1'D0' + D2'D1'D0 + D2'D1D0 = D2'$$

Wire D2' to the D input to implement the Bit 0 logic

6.

- a. Don't cares provide for circuit minimization beyond that possible if only 0 and 1 states were used.
- b. 20 MHz (Use scientific notation for these problems)
- c. To store one bit for use in sequential circuits
- d. Combinatorial: output = f(input)
Sequential: output = f(input, present state)
Combinatorial: adder, ROM, decoder, ALU
Sequential: counter, register
- e. To reduce the number of gates and increase the speed of logic
- f. Decoders always assert one output – based on input values

A	B	Output
0	0	0001
0	1	0010
1	0	0100
1	1	1000