

# John S. Seng

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## Education

Ph.D. in Computer Engineering, University of California, San Diego, June 2003.  
Dissertation: *Optimizing Processor Architectures for Power-Efficiency*  
Thesis adviser: Dean Tullsen.  
M.S. in Computer Engineering, University of California, San Diego, June 1999.  
B.S. in Computer Engineering, Northwestern University, June 1997.

## Academic Experience

Assistant Professor, California Polytechnic State University; September 2003 – present.

Research Assistant, University of California, San Diego; 1998 – 2003.  
Modified the SMTSIM architecture-level performance simulator to include an architecture-level power model. Utilized this power/performance simulator study architectural techniques which reduce the power consumption of general purpose microprocessors.

Teaching Assistant, Advanced Computer Architecture (graduate), University of California, San Diego; Spring 2002.

Teaching Assistant, Introduction to Computer Programming (undergraduate), University of California, San Diego; Winter 2002.

Teaching Assistant, Computer Architecture (undergraduate), University of California, San Diego; Winter 1999.

## Professional Experience

Intel Corporation, Santa Clara, CA; June 1999 – September 1999.  
Added an x86 instruction decoding front end to a RISC multithreading processor simulator (SMTSIM) - enabling the simulator to execute unmodified x86 Linux binaries. Modified the processor simulator to simulate x86 instructions as multiple RISC-like instructions. Incorporated an architecture-level power model, which was a part of the SimpleScalar simulator, into the x86 processor simulator.

Qualcomm Corporation, San Diego, CA; June 1998 – September 1998.  
Wrote test benches in VHDL for a base station ASIC for wireless signal demodulation. These test benches exercised small functional blocks and verified the blocks functioned according to the required specifications. Developed test programs in C which exercised portions of the ASIC via an embedded ARM core.

Compaq Computer Corporation, Houston, TX; June 1996 – August 1996.  
Tested remote paging and utilization monitors of Compaq server management software, Compaq Insight Manager version 3.10. This software allowed a single computer to monitor, over the network, the

health and status of multiple servers. Was involved in the testing and debugging of a beta version of software to automate software testing.

IBM Corporation, Costa Mesa, CA; June 1995 – September 1995.

Configured hardware and software (AIX 3.2.5 and 4.1.3) on RS/6000 machines and delivered them to customer locations. Compiled sales statistics used in determining regional workstation sales status and customer demand. Provided technical support at customer locations for RS/6000 servers and workstations.

## Awards

- IEEE Faculty Appreciation nomination 2006
- Outstanding CPE Instructor for 2005-2006, 2006-2007
- Outstanding Club Advisor, College of Engineering 2006
- UC MICRO fellowship, 1997-1998

## Professional Activities

Member of IEEE.

## Conferences and Workshops Attended

- The 2006 International Conference on Frontiers in Education: Computer Science and Computer Engineering, June 2006  
**Presented:** *PolyBot Board: a Controller Board for Robotics Applications and Education.*
- Second Value-Prediction and Value-Based Optimization Workshop, October 2004.  
**Presented:** *Exploring Perceptron-Based Register Value Prediction.*
- Power-Aware Computing Systems, December 2003.  
**Presented:** *Exploring the Potential of Architecture-Level Power Optimizations.*
- Semiconductor Research Corporation Contract Review, March 2004.  
**Invited Presentation:** *Power-Efficient Architecture of High Performance Processors.*
- International Symposium on Computer Architecture, June 2003.
- Workshop on Complexity-Effective Design, June 2003.
- Interaction between Compilers and Computer Architectures, February 2003.  
**Presented:** *The Effect of Compiler Optimizations on Pentium 4 Power Consumption*
- High Performance Computer Architecture, February 2003.
- International Symposium on Microarchitecture, December 2001.  
**Presented:** *Reducing Power with Dynamic Critical Path Information*
- International Symposium on Microarchitecture, December 2000.
- Kool Chips Workshop, December 2000.

- International Conference on Computer Design, September 2000.  
**Presented:** *Power-Sensitive Multithreaded Architecture*
- Workshop on Complexity-Effective Design, May 2000.  
**Invited Presentation:** *The Power-Efficiency of Multithreaded Architectures*
- International Symposium on Computer Architecture, May 2000.
- International Symposium on Computer Architecture, May 1999.  
**Presented:** *Storageless Value Prediction Using Prior Register Values*

### Invited Presentations

- “Power-Efficient Architecture of High Performance Processors”, Semiconductor Research Corporation Contract Review, March 2004
- “Reducing Processor Power Using Critical Path Information”, University of San Diego, Computer Science Colloquium, Winter 2003
- “The Power-Efficiency of Multithreaded Architectures”, Workshop on Complexity -Effective Design 2000

### Publications

- **J. Seng** and T. Norrie, “Sidewalk Following Using Color Histograms,” *The 2008 Consortium for Computer Sciences in the Colleges - Southwestern Regional Conference*, April 2008.
- T. Norrie and **J. Seng**, “Team-Based Project Design of an Autonomous Robot,” *The 2007 International Conference on Frontiers in Education: Computer Science and Computer Engineering*, June 2007.
- **J. Seng**, “PolyBot Board: a Controller Board for Robotics Applications and Education,” *The 2006 International Conference on Frontiers in Education: Computer Science and Computer Engineering*, June 2006.
- **J. Seng**, “PolyBot Board: A Robot Controller Board Using the Atmel ATmega32,” *Atmel Applications Journal*, June 2006. (editorial review, but not refereed)
- D. Franklin and **J. Seng**, “Experiences with the Blackfin Architecture for Embedded Systems Education,” *Twelfth Workshop on Computer Architecture Education*, June 2005.
- A. LeBeau, J. Fields, R. Lavinger, D. Franklin, and **J. Seng** , “Improving Non-Stationary Data Retrieval in Wireless Sensor Networks,” *Second International Workshop on Mobile and Wireless Ad Hoc Networking*, June 2005.
- **J. Seng** and D. Tullsen, “Architecture-Level Power Optimizations – What are the Limits?,” *Journal of Instruction Level Parallelism*, vol. 7, 2005.
- **J. Seng** and G. Hamerly, “Exploring Perceptron-Based Register Value Prediction,” *Second Value-Prediction and Value-Based Optimization Workshop*, October 2004.
- **J. Seng** and D. Tullsen, “Exploring the Potential of Architecture-Level Power Optimizations,” *Power-Aware Computing Systems*, December 2003. Also published in *Lecture Notes in Computer Science*, Volume 3164, December, 2004.
- **J. Seng** and D. Tullsen, “The Effect of Compiler Optimizations on Pentium 4 Power Consumption,” *Interaction between Compilers and Computer Architectures*, February 2003.

- **J. Seng**, E. Tune, and D. Tullsen, “Reducing Power with Critical Path Information,” *International Symposium on Microarchitecture*, December 2001.
- **J. Seng**, D. Tullsen, G. Cai, “Power Sensitive Multithreaded Architecture,” *International Conference on Computer Design*, September 2000.
- D. Tullsen and **J. Seng**, “Storageless Value Prediction Using Prior Register Values,” *International Symposium on Computer Architecture*, May 1999.

### Grant Activity

- **Awarded:** George Bekey (PI), Chris Clark, William Durgin, Art MacCarley, Robert MacDonald, Bryan Mealy, Saeed Niku, Mohammad Noori (PI), **John Seng**, Lynne Slivovsky, \$297,081 NSF REU Site Proposal, *Summer Internships In Robotics And Autonomous Systems*
- **Awarded: John Seng** (PI), \$5,000 Cal Poly Honors’ Research Project Grant 2006-2007, *Solar Powered Wireless Access Point*
- **Awarded:** John Seng (PI), Diana Franklin, \$40,000 Cal Poly C3RP ONR 2005-2006 Renewal Grant, *Large-Scale Distributed Wireless Networks*.
- **Awarded:** John Seng (PI), \$5,000 Cal Poly State Faculty Support Grant 2005-2006 Grant, *Using Dynamic Prediction to Eliminate Unnecessary Instructions in Programs*
- **Awarded:** John Seng (PI), Diana Franklin, \$45,000 Cal Poly C3RP ONR 2004-2005 Grant, *Large-Scale Distributed Wireless Networks*.

### Industrial Consulting

- Seven Pinnacles and Dilithium Networks Corp. – developed client/server software which supported the RMCP protocol for system status monitoring
- Seven Pinnacles and Intel Corp. – improved performance of a medical imaging application on a multi-core Intel processor
- Roxorgames Corp. – developed board layout and code for a multi-player wireless game controller
- ShipOK Corp. – developed a system architecture proposal for a fault-tolerant and high-availability system for package shipping